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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,763	SUGUMAR ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. Claims 1-19 are directed to methods for use in a processor. These methods comprise conditions for performing operations. The operations comprise substituting specifier for a greater width source register in claim 1, and other conditions for performing other operations in the claims that are abstract. This operations are abstract as they do not produce any tangible result. The operations for claims 1-19 do not transform any article or physical object to different state or thing or provide any tangible result. (see Diehr, 450 US. At 187,209 USPQ at 8; Benson 409 US at 71-72, 175 USPQ at 676-77; AT&T 172 F.3d at 1358-59, 50 USPQ2d at 1452.

4. Claims 2,8,16 include the a greater width source register is substituted for a lesser width source register is the greater width register onto which the lesser width source register is aliased. The substituting operation does not produce any tangible result and the aliasing of the register also does not produce any tangible result.

5. Claims 3,9,17 include substituting the greater width register includes an indication that a lesser width source register is to replace by a greater width register. The indication setting is setting a bit or bits does not produce any tangible result the interpretation of the meaning of the setting of a bit is abstract not tangible.

6. Claim 4 includes if dependency exists between lesser width producer instruction and a greater width consumer instruction substituting plural instructions for the greater width consumer instruction. This is a condition for performing an operation that does not produce any tangible result.

7. Claims 5,10,18,19 include plural instructions are claimed to merge registers and the merging of registers does not produce any tangible result. Also the mere execution of an instruction with a greater width or substitution of instructions using certain registers whether aliased or not does not necessarily produce any tangible result.

8. Claim 6 includes, determination of if dependency exist between a greater width instruction and a lesser width instruction that are either consumer and producer instructions substituting instructions. The mere substitution of instructions does not produce any tangible result.

9. Claim 7 includes stalling at least one instruction of a fetch group if a dependency exist between an instruction in the fetch group and both and active lesser width producer instruction and an active greater width producer instruction. The mere stalling of an instruction upon meeting a condition does not produce any tangibile result.

10. Claims 11 includes generating a first register mask identifying registers to be modified by lesser width instructions active in a pipeline; and generating a second register mask identifying a second register mask identifying registers to be modified by greater width instruction active in the pipeline. The mere masking bits in registers when a condition is met merely selects certain bits and this does not produce any tangible result.

11. Claim 12 includes the determining if a dependency exists includes comparing a lesser width register specifier of an instruction against the second register mask; and comparing a greater width register specifier of an instruction against the first register mask. This is merely a way to make a determination and does not produce any tangible result.

12. Claim 13 includes determining if a dependency exists includes determining if a greater width instruction in a fetch group modifies a lesser width source register specified by a younger instruction in the same fetch group. This is merely a determination and does not produce any tangible result.

13. Claim 14 includes determining if a dependency exists includes if a lesser width instruction in a fetch group modifies a greater width source register specified by a younger instruction in the same fetch group. This is merely a determination and no tangible result is produced.

14. Claim 15 includes, handling a register conflict between a first instruction specifying a greater width registers and a second register instruction specifying a lesser width source register...substituting for the execution the lesser width source register of the second instruction with a greater width source register specifier. The provides for the substituting of registers which does not provide for any tangible result.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-4, 6,8,9,15,16,17,20,22,23,31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kahle (patent No. 5,732,005).

17. Kahle taught the invention substantially as claimed including a data processing ("DP") system comprising:

18. As per claims (1,6,15,20,23,31) Kahle taught if a dependency exists between a greater width producer instruction and a lesser width consumer instruction, substituting for execution a greater width source register specifier for a lesser width source register specified by lesser width consumer instruction (e.g., see col. 4, lines 7-59)[retrieving the data as an emulated double precision data when the operand to be retrieved in a single precision memory location is larger than the single precision range and has been stored as an emulated double precision data. Also Kahle taught substituting an emulated double precision specifier (e.g., see col. 5, line 52-col. 6, line 23)].

19. As per claim 2,8,9,16,31 Kahle taught the greater width source register substituted for the lesser width source register is the greater width register onto which the lesser width source register is aliased, and setting an indication (e.g, see col. 2, lines 39-55 and col. 4, lines 31-59).

20. As per claim 3,17,22 Kahle taught substituting the greater width register includes setting an indication that the lesser width source register is to be replaced by the greater width register (e.g., see col. 2, lines 39-55 and col. 4, lines 31-59).

21. As to the limitations of claim 4,6,31 Kahle taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, substituting plural instructions (emulation routine for double precision instruction) for the greater width instruction [a double precision operation is performed on data stored by a single precision operation as single precision data using emulation routines] (e.g., see col. 1, lines 39-55 and col. 5,line 52-col. 6,line 22).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 5,7,10,18,19,21,24,32,33,34,35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle (patent No. 5,732,005).

24. As per claim 1,6,15,20, Kahle taught if a dependency exists between a greater width producer instruction and a lesser width consumer instruction, substituting for execution a greater width source register specifier for a lesser width source register specified by lesser width consumer instruction (e.g., see col. 4, lines 7-59)[retrieving the data as an emulated double precision data when the operand to be retrieved in a single precision memory location is larger than the single precision range and has been stored as an emulated double precision data. Also Kahle taught substituting an emulated double precision specifier (e.g., see col. 5, line 52-col. 6, line 23)].

25. As per claim 2,8,9,16, Kahle taught the greater width source register substituted for the lesser width source register is the greater width register onto which the lesser width source register is aliased, and setting an indication (e.g, see col. 2, lines 39-55 and col. 4, lines 31-59).

26. As per claim 3,17,22 Kahle taught substituting the greater width register includes setting an indication that the lesser width source register is to be replaced by the greater width register (e.g., see col. 2, lines 39-55 and col. 4, lines 31-59).

27. As to the limitations of claim 4,6, Kahle taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, substituting plural instructions (emulation routine for double precision instruction) for the greater width instruction [a double precision operation is performed on data stored by a single precision operation as single precision data using emulation routines] (e.g., see col. 1, lines 39-55 and col. 5,lines 52-col. 6,line 22).

28. As to the limitation of claim 4, Kahle taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, substituting plural instructions (emulation routine for double precision instruction) for the greater width instruction [a double precision operation is performed on data stored by a single precision operation as single precision data using emulation routines] (e.g., see col. 1, lines 39-55 and col. 5,lines 52-col. 6,line 22).

29. As per claim 5,10,18,19,24,33 Kahle did not specify the individual instructions for the emulation of the double precision instructions. However Kahle taught the operation of merging single precision register that are mapped to act as a double precision register and performing double precision operations comprising plural operands on the data. Therefore one of ordinary skill would have been motivated to provide separate instructions for combining each of the single precision operation to provide the plural double precision operands and an instruction to execute the double operation on the double precision data and designate first and second temporary registers as source register of the double precision instruction (e. g., see col. 5, lines 52-col. 6,line 22).

30. As per claim 7,21,32 Kahle taught the double precision operations that are emulated take longer that the single precision operations (e.g., see col. 4, lines 7-15). The stalling of processor execution of a stream of instruction when an instruction required emulation was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to stall the instructions that including fetching when the was a dependency on an instruction that required emulation (i.e. double precision instruction) at least to ensure the instruction that was dependent properly accessed the data. This emulation would have prevented that original instruction from being delivered.

31. As to the limitations of claim 13, 14,34,35 the fetching of data in groups or blocks was well known in the art at the time of the claimed invention at least because the instructions in the same group or block would be more likely to be to be used with a fetched instruction. Therefore it would have been obvious to one of ordinary skill that at

least some instructions in the Kahle sytem comprising greater and lesser width instructions that were tested as to their dependency would have been fetched in a group.

32. Claims 11,12,13,14,are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle as applied to claims 1-10 above, and further in view of Yeager (patent No. 6,216,200).

33. Kahle taught substituting the greater width register includes setting an indication that the lesser width source register is to be replaced by the greater width register (e.g., see col. 2, lines 39-55 and col. 4, lines 31-59).

34. Yeager taught (claims 11,12,) generating a first register mask identifying registers to be modified by instructions active in a pipeline and generating a second register mask identifying registers to be modified by greater width instructions active in the pipeline, Comparing the register specifier against a second mask and comparing a register specifier against a first register mask (e.g, see figs. 13a,13b,14,25a,25b). Considering Yeager teachings of masks for determining dependency and the Kahle teachings of dependency between single and double precision instructions one of ordinary skill would have been motivated generate register masks and to compare the double and single with register specifiers against masks (e.g., see col. 5, line 35-col. 6, line 34).

35. As to the limitations of claim 13, 14, the fetching of data in groups or blocks was well known in the art at the time of the claimed invention at least because the instructions in the same group or block would be more likely to be to be used with a

fetched instruction. Therefore it would have been obvious to one of ordinary skill that at least some instructions in the Kahle sytem comprising greater and lesser width instructions that were tested as to their dependency would have been fetched in a group.

36. It would have been obvious to one of ordinary skill to combine the teachings of Kahle and Yeager. Both references were directed toward the processing of instructions that had dependencies on other instructions . One of ordinary skill would have been motivated to incorporate the Yeager teachings of masks for comparing register modifiers at least to provide quick comparison of the register masks and providing quick determination of dependencies..

37. Claims 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager (patent No. 6,216,200) in view of Kahle.

38. Yeager taught (claim 25) generating a first register mask identifying registers to be modified by instructions active in a pipeline and generating a second register mask identifying registers to be modified by greater width instructions active in the pipeline, Comparing the register specifier against a second mask and comparing a register specifier against a first register mask (e.g, see figs. 13a,13b,14,25a,25b). Considering Yeager teachings of masks for determining dependency and the Kahle teachings of dependency between single and double precision instructions one of ordinary skill would have been motivated generate register masks and to compare the double and single with register specifiers against masks (e.g., see col. 5, line 35-col. 6, line 34).

39.

40. Yeager did not teach (claim 25) plural counters (count) to track the number of instructions in the active pipeline plural mask registers and logic to compare source and destination registers (e.g., see fig. 13a). However Kahle taught instructions with different precisions. Considering the instructions with different precision in Kahle one of ordinary skill would have been motivated to provide plural counters with at least one for single precision instructions and one for double precision instructions.

41. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Yeager and Kahle.. Both references were directed toward the processing of instructions that may be dependent on other instructions. One of ordinary skill would have been motivated to incorporate the Kahle teachings of plural width instructions that had dependencies at least to provide for more flexible processing for variable length data.

42. As per claim 26, Kahle taught the double precision operations that are emulated take longer that the single precision operations (e.g., see col. 4, lines 7-15). The stalling of processor execution of a stream of instruction when an instruction required emulation was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to stall the instructions that including fetching when the was a dependency on an instruction that required emulation (i.e. double precision instruction) at least to ensure the instruction that was dependent properly accessed the data. This emulation would have prevented that original instruction from being delivered.

43.

44. As per claim ,27 Kahle taught if a dependency exists between a greater width producer instruction and a lesser width consumer instruction, substituting for execution a greater width source register specifier for a lesser width source register specified by lesser width consumer instruction (e.g., see col. 4, lines 7-59)[retrieving the data as an emulated double precision data when the operand to be retrieved in a single precision memory location is larger than the single precision range and has been stored as an emulated double precision data. Also taught substituting an emulated double precision specifier (e.g., see col. 5, line 52-col. 6, line 23)].

45. As per claim 28, Kahle did not specify the individual instructions for the emulation of the double precision instructions. However Kahle taught the operation of merging single precision register that are mapped to act as a double precision register and performing double precision operations comprising plural operands on the data. Therefore one of ordinary skill would have been motivated to provide separate instructions for combining each of the single precision operation to provide the plural double precision operands and an instruction to execute the double operation on the double precision data and designate first and second temporary registers as source register of the double precision instruction (e. g., see col. 5, lines 52-col. 6,line 22).

46. As to the limitations of claim 29,30 the fetching of data in groups or blocks was well known in the art at the time of the claimed invention at least because the instructions in the same group or block would be more likely to be to be used with a fetched instruction. Therefore it would have been obvious to one of ordinary skill that at least some instructions in the Kahle system comprising greater and lesser width

instructions that were tested as to their dependency would have been fetched in a group.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eisen (patent No. 5,678,016) disclosed a system for managing execution of an instruction that determine subsequent to dispatch if an instruction is subject to serialization (e.g., see abstract).

Leung (patent No. 5,790,827) disclosed a method for dependency checking (e.g., see abstract).

Putrino (patent No. 5,805,475) disclosed a load-store unit and method of loading and storing single-precision floating-point registers in a double-precision architecture (e.g., see abstract).

Panwar (patent No. 6,094,719) disclosed a system for reducing data dependent conflicts by converting single precision instructions into microinstruction using renamed phantom registers in a processor having double precision registers (e.g., see abstract).

Prabhu (patent No. 6,463,525) disclosed merging single precision floating point operands (e.g., see abstract).

Colwell (patent No. 5,446,912) disclosed partial width stalls within register alias table (e.g., see abstract).

Bluhm (patent No. 5,630,149) disclosed pipelined processor with register renaming hardware (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER